The basic mechanisms for dealing with ESD are to create an environment where the charge is spread out as quickly as possible, where circuits are designed to couple less energy, and where charge that enters the circuit is shunted away from sensitive components. Spreading the charge delivered by an ESD event minimizes concentrated currents at any one point and reduces the magnitude of resultant electromagnetic fields. The same grounding techniques used for EMC apply to ESD protection, because they establish continuous low-inductance grounded surfaces. Fewer gaps in a metal chassis are less restrictive to a high-frequency ESD pulse. Well grounded cables improve a system's ESD protection, because energy that makes its way onto a cable's shield can be rapidly conducted by the metal chassis instead of coupling onto the inner conductors and making its way into the circuit. A high-quality shield makes positive electrical contact with the metal chassis in many places—ideally continuous contact around its perimeter. In contrast, a thin wire, or pigtail, connecting a cable's shield to the chassis severely degrades the quality of the ground connection at high frequencies because of its high inductance. EMC and ESD engineers strictly avoid pigtails for this reason.

Objects such as switches that protrude from an enclosure should be well grounded to that enclosure so that charge can be dissipated by the enclosure rather than through internal circuits. Remember that the charge delivered by an ESD event must eventually find its way to ground, and it will find the path of least inductance to get there. You want that path to be through a system's ground structure instead of through its circuitry.

Despite its common use in portable consumer electronics, plastic is a less desirable chassis material as compared to metal, because it is unable to dissipate ESD on its own and it does not attenuate electromagnetic fields. Thin metallic coatings can help substantially with ESD and EMC issues, because conductive surface area is important at high frequencies because of skin effect. However, such coatings add to the cost of a product and may begin to flake off or wear over time.

The rules learned from EMC design—minimizing loop area with low-impedance transmission lines and ground planes—apply to ESD protection, because less energy will be coupled by a smaller loop. Older style single- and double-sided PCBs are more sensitive to ESD, because they typically have larger return path loops as a result of their lack of a continuous ground plane. Using wide traces to reduce the inductance of ground and power distribution can improve the situation somewhat, but there is a practical limit to how wide the power traces can become before routing other signals becomes impossible. One can minimize trace lengths by keeping passive components such as bypass capacitors and pull-up resistors close to ICs, and this may be one of the more significant circuit layout steps that can be taken to minimize ESD sensitivity in single- and double-sided PCBs.

A well designed system should restrict the bulk of potentially destructive ESD exposure to I/O circuitry. Inductive coupling can occur to any part of the circuit but, depending on distances and quality of PCB grounding, inductive coupling effects on internal digital buses may be mild enough to cause either no problems or only soft errors in which, for example, a memory read might return wrong data during the ESD event. Soft errors can certainly be problematic, because memory can get corrupted, or a microprocessor can crash after reading a corrupted instruction. If a system's operational environment subjects it to occasional ESD events, and inductive coupling is sufficient to cause soft errors, the solution is to somehow modify the circuit to reduce coupling or to become tolerant of soft errors via the use of redundancy or error-correcting codes. Inductive coupling might be reduced with multiple layers of shielding and better grounding. Redundant algorithms and error coding can take the pessimistic view that soft errors are expected every so often and therefore explicitly deal with them.

I/O components usually bear the brunt of ESD, because they must inherently connect to the outside world. If an ESD event occurs on an RS-232 cable, the RS-232 transceiver is going to be the first semiconductor to see that spike. This is where blocking and shunting high-frequency energy becomes important. A basic passive filter can be employed to attenuate high-frequency ESD events on an individual wire. Figure 18.18 shows several variations of ESD filtering. Many other solutions

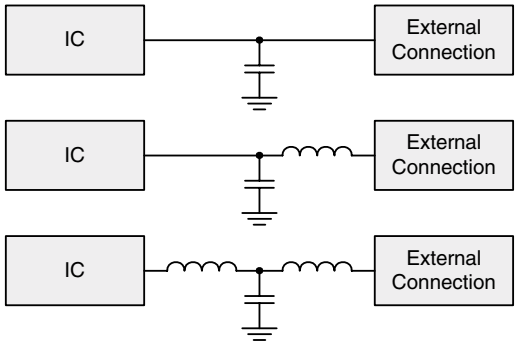

FIGURE 18.18 Various ESD filters.

are possible. Some scenarios rely on inductance of the wiring in combination with a single high-frequency capacitor to attenuate ESD. Others explicitly insert ferrite beads to add inductance to the circuit.

The example circuits shunt ESD to logic ground, but the ideal situation is to shunt the energy to chassis ground. Chassis ground presumably would have a less direct connection to the IC being protected. However, there is added complexity in separating ground regions on a circuit board, and the possibility then arises for unintended return paths to cause EMC problems. If logic ground is well attached to chassis ground at the connector, a low-inductance loop is formed from the cable, through a shunt capacitor, to logic ground, and finally to chassis ground. Inserting an inductor between the external cable connection and the shunt capacitor increases the inductance of this path, but the idea is to make this path less desirable for ESD so that it finds a lower-inductance path to ground and bypasses the wire leading to the IC altogether. Any ESD that makes it through the first inductor must be immediately presented with a low-inductance path to ground so that it does not conduct through the IC instead. A low-inductance path is created using a high-frequency surface mount capacitor connected to the inductor and ground nodes with the shortest traces possible. This filtering not only improves ESD immunity, it also reduces unwanted emissions that may cause regulatory compliance problems.

An additional ESD protection mechanism is a high-speed Zener diode that can respond quickly enough to clamp a node's voltage and shunt excess energy to ground. This semiconductor solution has the benefit of not being a lowpass filter, so it is therefore more applicable to high-speed interfaces such as Ethernet. Speed is a critical specification for an ESD clamping diode, because the initial ESD pulse typically ramps in less than 1 ns. A slow diode will add little or no ESD protection. Clamping diodes may be implemented with discrete components on a circuit board and are also implemented on some interface ICs for enhanced ESD tolerance. RS-232 transceivers are available from companies such as Linear Technology and Maxim with integrated shunt diode structures that provide up to 15 kV of protection, which is a standard threshold for ESD tolerance. RS-232 transceivers are prime candidates for ESD hardening, because the interface has become so inexpensive and common that it is used in many abusive environments. There are also ESD protection products specifically designed for high-speed interfaces, including Ethernet, that implement the same type of technology. They are made by companies such as California Micro Devices, Philips, and Semtech.